Design of 8-bit microprocessor using Verilog (SAP-1 architecture)

INTRODUCTION

- The Simple-As-Possible (SAP)-1 computer is a very basic model of a microprocessor explained by Albert Paul Malvino1.
- The SAP-1 design contains the basic necessities for a functional Microprocessor.
- Its primary purpose is to develop a basic understanding of how a microprocessor works, interacts with memory and other parts of the system like input and output. The instruction set is very limited and is simple.

The features in SAP-1 computer are

- W bus - A single 8 bit bus for address and data transfer.
- 16 Bytes memory (RAM).
- Registers are accumulator and B-register each of 8 bits.
- Program counter – initializes from 00H(0d) to FFH(15d) during program execution.
- Memory Address Register (MAR) to store memory addresses.
- Adder/Subtracter for addition and subtraction instructions.
- A Control Unit.
- A Simple Output.
- 6 machine reserved for each instruction.

The instruction format of SAP-1 Computer is

(XXXX) (XXXX)

the first four bits make the opcode while the last four bits make the operand(address).

SAP-1 instruction set consists of following instructions

Mnemonic	Operation	OPCODE
LDA	Load addressed memory contents into accumulator	0000
ADD	Add addressed memory contents to accumulator	0001
SUB	Subtract addressed memory contents from accumulator	0010
OUT	Load accumulator data into output register	1110
HLT	Stop processing	1111

Machine cycle & Instruction cycle

- SAP1 has six T-states (three fetch and three execute cycles) reserved for each instruction. Not all instructions require all the six T-states for execution. The unused T- state is marked as No Operation (NOP) cycle.
- Each T-state is called a machine cycle for SAP1. A ring counter is used to generate a T-state at every falling edge of clock pulse. The ring counter output is reset after the 6th T-state.
- FETCH CYCLE – T1, T2, T3 machine cycle
- EXECUTE CYCLE - T4, T5, T6 machine cycle

Architecture

1. Program Counter (PC)

- implemented in “pc.v” file
- It counts from 0000 to 1111 and it signals the memory address of next instruction to be fetched and executed

2. Input and MAR (MAR)

- implemented in “inputMAR.v” file
- During a computer run, the address in PC is latched into Memory Address Register (MAR).

3. RAM

- implemented in “mem16k.v” file
- the program code to be executed and data for SAP1 computer is stored here.
- During a computer run, the RAM receives 4-bit addresses from MAR and a read operation is performed. Hence, the instruction or data word stored in RAM is placed on the W bus for use by some other part of the computer.
- It is asynchronous RAM, which means that the output data is available as soon as valid address and control signal are applied

4. Instruction Register (IR)

- implemented in “ir.v” file
- IR contains the instruction (composed of OPCODE+ADDRESS) to be executed by SAP1 computer.

5. Controller- Sequencer

- implemented in “cu.v” file
- it generates the control signals for each block so that actions occur in desired sequence. CLK signal is used to synchronize the overall operation of the SAP1 computer.
- A 12 bit word comes out of the Controller-Sequencer block. This control word determines how the registers will react to the next positive CLK edge.

6. Accumulator • implemented in “accumulator.v” file

- it is a 8 bit buffer register that stores intermediate results during a computer run.
- It is always one of the operands of ADD,SUB and OUT instructions.

7. Adder-Subtracter

- implemented in “addersubtracter.v” file
- it is a 2's complement adder-subtractor
- this module is asynchronous (unclocked), which means that its contents can change as soon as the input words change

8. B Register

- implemented in “register.v” file
- it is 8 bit buffer register which is primarily used to hold the other operand (one operand is always accumulator) of mathematical operations.

9. Output Register

- this registers hold the output of OUT instruction.

10. Binary Display

- it is a row of eight LEDs to show the contents of output register

OBJECTIVES

- By using PIC 16F877,the latest microcontroller as CPU, this project has vast applications in FDM (frequency division multiplexing) and TDM (time division multiplexing) and also in separate spectrums like CDMA,TDMA,FDMA.

- As there is no analogue measurement, so this device is used in all technical institutions,colleges,laboratories for the direct digital display of Time period, Frequency, T ON, and T OFF.

- It is used in everywhere ,where T ON and T OFF needed to be measure.

BENEFITS OF THE PROJECT

- PIC(programmable interrupt controller) as CPU.
- Auto ranging.
- Simple to use with memory buttons.
- Frequency measurement from 1 Hz to 99 Hz.
- Time period measurement from 0.001 ms to 1s.
- T ON measurement from 0.001 ms to 1s.
- T OFF measurement from 0.001 ms to 1s.
- Accurate measurement with ±1 Hz error.
- Extendable range to ultra high frequency. super high frequency and extremely high frequency.
- Smaller in size.
- Less costly and portable.
- Faster in operation.
- Both DTM and DFM are achieved.
- Used by R & D people.
- Used by private channel organization and in HAM radio.

TOOLS AND TECHNIQUES

- PIC 16F877 microcontroller
- Crystal Oscillator (20MHz).
- Driver circuit (ULN 2003)
- Seven Segment Display
- Switching Buttons
- 5V power supply

FUTURE WORK

- The concept of SAP1 is very simple, the knowledge gained while designing it can be extended to design of more complex microprocessors.

CONCLUSION

- We successfully designed a 8-bit microprocessor based on SAP1 architecture and verified it's operations in Verilog.