Faculty of Engineering and Applied Science
Memorial University of Newfoundland
ENGI 3861 - Digital Logic
Fall 2017

Laboratory 1:
CMOS Circuits and Combinational Circuit Design

Pre-lab

All students must review the complete lab prior to the lab period. Each group must complete all sections marked as "PRE-LAB". The pre-lab will be checked by a TA at the start of the lab. If a group's pre-lab work is not complete, the group may not be allowed to complete the experiment.

Lab Report

Each group is expected to complete a lab report. At the end of the lab, hand in the lab report. The report should include the pre-lab along with the lab observations and comments requested. Where indicated, demonstrate the correct operation of your circuit to a TA and have them sign your lab report.

1. Introduction

The purpose of this lab is (1) to investigate the electrical characteristics of CMOS gates and (2) to apply combinational logic design techniques to the implementation of a simple elevator controller.

2. Characteristics of CMOS Gates

(a) Complete this part as **PRE-LAB**, using the data sheets posted on the course website:

(i) For SN74HC00 and SN74HC04, determine the minimum acceptable values for V_{IH} and V_{OH} using V_{CC} = 4.5 V and output current of 20 μA. What are the maximum acceptable values for V_{OL} and V_{IL} under the same test conditions? Compute the noise margins.

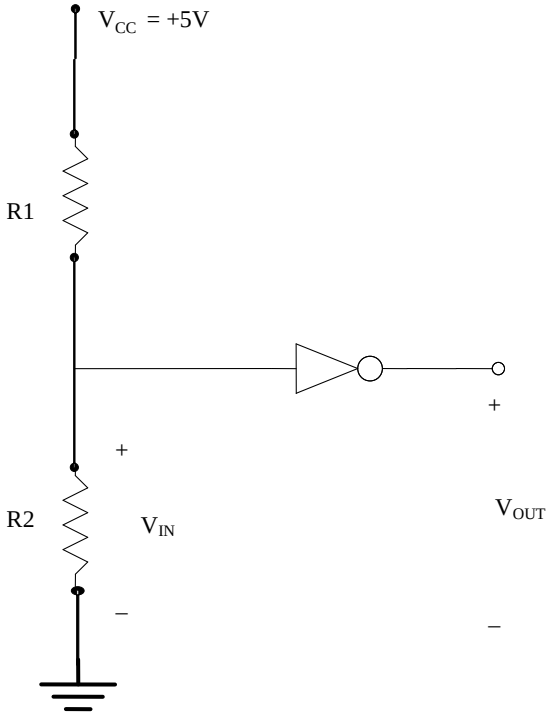
(ii) For SN74HC00 and SN74HC04, determine the specifications for propagation delay for high-to-low and low-to-high transitions. Assume V_{CC} = 4.5 V.

(b) In this section of the experiment, you will investigate the transfer characteristic (i.e., V_{IN} vs. V_{OUT}) of a CMOS inverter by measuring voltages in the circuit given below containing an inverter and two resistors. The concept is to measure the output voltage for a given input voltage, using a voltage divider circuit to set the input voltage to a level between 0V and 5V. As **PRE-LAB** compute the expected input voltage for each set of resistance values of R1 and R2 indicated in the table

below. (Note that, for CMOS, it is reasonable to assume that the input resistance of the gate is infinite.)

In the lab, construct the circuit with an SN74HC04 device for each scenario of R1 and R2 indicated in the table below. Remember to connect GND and V_{CC} pins of the IC. Use the provided set of resistors (with values 10 kΩ, 2 kΩ, 1 kΩ, 510 Ω, and 100 Ω) to configure the resistance values. Where necessary, connect multiple resistors in series to get the require value. ***Using the digital multimeter, measure and record the voltages at the input to the inverter and the output of the inverter. Complete a table which includes resistance, expected input voltage, measured input voltage, and measured output voltage for each set of resistance values. Using graph paper or quad paper, plot of the transfer characteristic of the CMOS inverter. Comment on the nature of the resulting graph.***

R1	R2
1 kΩ	∞ (open)
1 kΩ	10 kΩ
1 kΩ	4 kΩ
1 kΩ	3.51 kΩ
1 kΩ	3 kΩ
1 kΩ	2.51 kΩ
1 kΩ	2 kΩ
1 kΩ	1.51 kΩ
1 kΩ	1 kΩ
1 kΩ	510 Ω
1 kΩ	100 Ω



3. Design of an Elevator Controller

An elevator services three floors: ground (G), floor 1, and floor 2. The elevator controller receives inputs, S1 and S2, from a sensor that provides the identity of the current floor, and inputs R1 and R2, from another circuit that processes the floor requests and gives the destination floor. The elevator controller circuit (1) operates the elevator motor, which moves the elevator, or does not move the elevator, via an ENABLE output signal, and (2) moves the elevator up or down via a DIRECTION output signal.

The specifications for the sensor, floor request circuit, and the elevator motor control are given below. Note that S1, S2, R1, and R2 are inputs to the controller and ENABLE and DIRECTION are output signals sent to the motor to control its behaviour.

Sensor Specification		
Current Floor	**S1**	**S2**
G	1	1
1	1	0
2	0	1

Floor Request Specification		
Destination Floor	**R1**	**R2**
G	1	1
1	1	0
2	0	1

Motor Specification	
ENABLE	**Meaning**
0	stop motor, open door
1	close door, activate motor
DIRECTION	**Meaning**
0	if motor activated, go down one floor
1	if motor activated, go up one floor

[Complete the following design as PRE-LAB.]

Design the elevator controller circuit as a combinational logic circuit that produces the appropriate ENABLE and DIRECTION signals to operate the elevator. Your final circuit design should use only NAND gates and inverters.

Some hints:

(a) Begin by drawing a block diagram showing the relationships between the sensor, floor request circuit, motor and the elevator controller circuit.

(b) Develop a truth table of the controller outputs (ENABLE and DIRECTION) as a function of the inputs S1, S2, R1, and R2. Since you have not been given the explicit output for some inputs, to minimize the number of gates in the circuit, it is desirable to mark these outputs as “don’t care”, denoted by “X” and meaning that either a 0 or 1 is acceptable. This will give more flexibility when minimizing using a Karnaugh map.

(c) Use K-maps to minimize your circuit into a sum-of-product form.

(d) Draw your circuit using AND-OR logic, then convert the diagram into an equivalent circuit using only 2-input NAND and NOT gates.

(e) When you are confident that the design is correct, mark onto your diagram chip and pin numbers for the various gates in your circuit. This will be very helpful in constructing and debugging the circuit in the lab.

Once you have completed your circuit design, reflect on the following scenario:
To obtain certification from the building safety bureau, you need to provide a statement on the user safety and emergency failsafe capabilities of your circuit. Take a look at your design again and comment on what happens when inputs are accidently shorted to ground. State how you would get around any problem that might occur in this circumstance. (You do not have to redesign your circuit to do this.)

4. Circuit Implementation and Debugging

[Complete this section in the lab.]

In the lab, construct the elevator controller circuit based on only NANDs and NOTs on the breadboard. Connect the inputs to switches and the outputs to LEDs for ease of testing. Test your circuit to ensure that it satisfies the specification. You will probably find the logic probe very useful for debugging. Once you are sure that your circuit is working as expected, demonstrate the correct operation of the circuit to a TA and have them sign your lab report.

5. Report Submission

Submit your lab report once your circuit has been verified by the TA. The lab report should include:

(a) results and comments from Section 2
(b) details of the elevator controller design, implementation, and testing, including
  (i) a full description of the elevator controller design (including block diagram, truth table, K-maps, circuit diagrams, and appropriate comments)
  (ii) a discussion of any problems encountered during the elevator controller implementation in the lab and the methods used to overcome the problems