Faculty of Engineering and Applied Science
Memorial University of Newfoundland
ENGI 3861 - Digital Logic
Fall 2017

Laboratory 3:
Flip-Flops and Sequential Circuits

Pre-lab:
The pre-lab will be checked by a TA at the start of the lab. ***If a group's pre-lab work is not complete, the group will be given a major mark penalty.***

Lab Report:
Each group is expected to complete a lab report. At the end of the lab, hand in the lab report, which should include the pre-lab, along with the lab observations and comments requested. Where indicated, demonstrate the correct operation of your circuit to a TA and have them sign your lab report.

1. Introduction

The purpose of this lab is to become familiar with the internal structure of flip-flops and with their use in sequential logic circuits.

2. D Latches and Flip-Flops

In this section of the lab, you will construct both a D latch and a positive edge-triggered D flip-flop and verify their functionality.

D Latch

[Pre-lab] Draw the circuit diagram for the D latch with an enable (EN), based on NAND gates. Label the IC pin numbers on the diagram for ease of construction during the lab. In the lab, it will be necessary for you to test the correct functionality of your circuit by applying appropriate values to the inputs D and EN and observing the resulting outputs, Q and QN. Assuming that D and EN are connected to switches, develop a strategy for testing the circuit. Your strategy should include a full set of test cases that will cover all possible scenarios. Prior to the lab, construct the circuit on the digital board. Using switches for inputs D and EN, verify the correct functionality of the circuit based on the tests developed. Construct and test a second D latch. Do not dismantle the D latches, as you will need them for the next section.

D Flip-Flop

[Pre-lab] Draw the logic diagram for a positive edge-triggered D flip-flop using two D latches in series. The flip-flop does not need to have an enable. In the lab, it will be necessary for you to test the correct functionality of your circuit by applying appropriate values to the inputs D and the clock (CLK) and observing the resulting outputs, Q and QN. Assuming that input D is connected to a switch and CLK is connected to a pulse generator (i.e., one of the push buttons on the board – experiment with them to determine how they work!), develop a strategy for testing the circuit. Your strategy should include a full set of test cases that will cover all possible scenarios.

[In the lab] Connect the two D latches constructed in the pre-lab to form a master-slave D flip-flop. Using your test strategy, verify the correct functionality of the circuit. Demonstrate your circuit to a TA and have them sign your lab report.

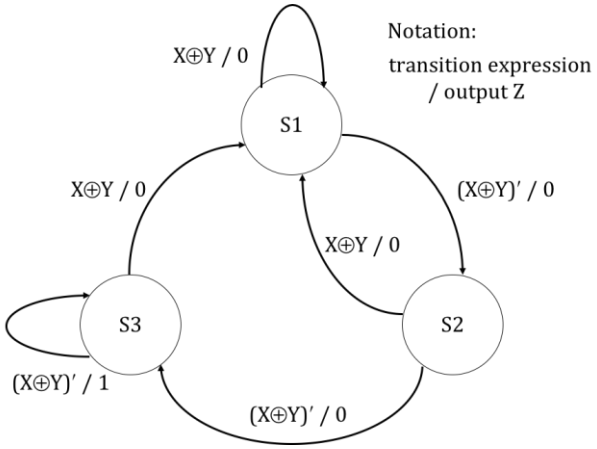
3. Design of Sequential Circuits

The 7474 IC contains two positive edge-triggered D flip-flops with asynchronous clear and preset inputs. In this section of the lab, the D flips-flops will be used in the implementation of a state machine.

[Pre-lab] Design a sequential circuit to implement the following state diagram, which uses transition expressions on the transition arcs. For convenience, use an encoding for the state that is the binary representation of the state number. In your analysis and the resulting circuit, label the input signals as X and Y and the output signal as Z. Your circuit should contain only D flip-flops and any gates that are appropriate and available. For convenience when implementing the design, try to use as few gates as possible. Indicate all IC pin numbers on your logic circuit diagram for ease of construction and troubleshooting in the lab.

[Pre-lab] In words, describe the behaviour of the circuit as seen by an external device. You may assume that the system is initialized to state S1. Note that an external device would be aware of all inputs and outputs of the system, but would have no knowledge of the internal states of the system. Draw a timing diagram (neatly on quad or graph paper) to illustrate the behaviour of the circuit over a range of states and inputs. Make sure the diagram traverses all arcs at least once.

[In the lab] Wire this circuit and verify its correct functioning based on the timing diagram developed in the pre-lab. Connect the flip-flop clear and preset inputs to switches on the board so that you can set the initial state to S1 as desired. Demonstrate your design to a TA and have them sign your lab report.



4. Report Submission

Submit your lab report once your circuits have been verified by the TA. The lab report should include:

(a) the pre-lab including any appropriate state tables, transition tables, K-maps, circuit diagrams, etc.
(b) recorded outcomes of tests and associated comments
(c) a discussion of any problems encountered during the implementation in the lab and the methods used to overcome the problems