Faculty of Engineering and Applied Science
Memorial University of Newfoundland
ENGI 3861 - Digital Logic
Fall 2017

Laboratory 5:
Digital System Design

Pre-lab:
Each group is required to complete the pre-lab sections prior to the lab period. The pre-lab will be checked by a TA at the start of the lab. If a group's pre-lab work is not complete, students may not be allowed to complete the lab and a severe mark penalty will be applied.

Lab Report
Each group is expected to complete a lab report. At the end of the lab, hand in the lab report, which should include the pre-lab, along with the lab observations and comments requested. Where indicated, demonstrate the correct operation of your circuit to a TA and have them sign your lab report.

1. Introduction

The purpose of this lab is to become familiar with digital system design, using state machines and common devices such as counters and shift registers.

2. Serial Transmitter

In this lab, you will design a serial transmitter circuit that takes an 8-bit data word in parallel as input, when an input control signal (SEND) goes high, and serially outputs the word (i.e., one bit during each clock cycle) to a single transmission line. Transmission of a word begins with the least significant bit, preceded by a high "start" bit and terminated by at least two low "stop" bits.

The transmission line should have a low signal level, until the start of the transmission of an 8-bit word (as indicated by the start bit which is a high level). Note that each word on the transmission line must be separated by at least two bit times of low (i.e., the stop bits), prior to the arrival of the next start bit.

You may assume that SEND is set low prior to the completion of the transmission and re-asserted when the next data word is available to transmit.

[Prelab]

Design 1 - Basic Transmitter
Design the transmitter using appropriate MSI components such as counters (eg. 74163) and shift registers (eg. 74165). Refer to the course web site for the data sheets of components that you can use for your design. In your lab report, be sure to include all aspects of your design, including an I/O diagram and block diagram of the full system, state diagram of the control unit, state table, transition/excitation table, and logic diagram of your design. Also, be sure to develop a timing diagram to be used in testing your circuit. The timing diagram sequence should thoroughly exercise your design and should be done neatly on graph or quad paper. *State any assumptions that you have had to make about the functionality of the system.*

Design 2 - Transmitter with Parity

To detect errors, consider an additional specification that the 8^{th} bit of the word transmitted is to be set as the parity bit (using even parity), which means that this bit is overwritten from its inputted value and set to ensure that the transmitted word has even parity. Modify your design to incorporate the required functionality to achieve this. Consider the possibility in your design of computing the parity bit serially as the bits are being transmitted out, thereby using only one two-input XOR gate (in addition to other components). Your modified design description should include a new block diagram, state diagram, state table, transition/excitation table, and logic diagram for the design. You do not need to provide a timing diagram and you will not be implementing this new design on the board.

[In the lab]

Implement "Design 1 - Basic Transmitter" (without parity) using the necessary components on the digital logic board. Verify the correct functionality of your circuit based on your timing diagram and record the results of your testing. When you are certain that your circuit is functioning correctly, demonstrate your circuit to a TA and have them sign your lab report.

3. Report Submission

Submit your lab report once your circuit has been demonstrated to (and your report signed by) the TA. The lab report should include:

(a) the pre-lab including all design information, logic diagrams, and timing diagram
(b) recorded outcomes of tests and associated comments
(c) a discussion of any problems encountered during the implementation in the lab and the methods used to overcome the problems